Low Temperature Double-Exposed Polyimide/Oxide Dielectric for VLSI Multilevel Metal Interconnection

THOMAS E. WADE, SENIOR MEMBER, IEEE

Abstract—**By use of a double-exposed (double-etch) low temperature polyimide/oxide process, the packing density for both first and second level metal interconnection can be improved by some 35 percent and 30 percent, respectively, in the vicinity of the via. Moreover, the complete interconnect process may be realized at temperatures below 300°C. Since polyimide can be applied in thick layers having negligible (tensile) stress, a planar surface results and also parasitic lead capacitances may be considerably reduced. This process is also amenable to either wet chemical or dry plasma processing.**

INTRODUCTION

As THE DENSITY of very large scale integrated (VLSI) circuits continues to increase for decreasing design dimensions, resulting from improved lithography and associated patterning technology, it becomes imperative that a multilevel interconnection system be employed which can be realized using low temperature processing techniques. The dielectric material must be of good quality (i.e., high dielectric strength and resistivity; low pinhole density, particulates, and dielectric constant; good thermal expansion coefficient, etc.) and one which can be deposited at low temperatures (to prevent lateral and outdiffusion of dopant impurities, degradation of radiation-hard characteristics, and reduced hillock formation). It is also desirable to use a dielectric material which will minimize stray interconnect capacitance effects and render a planar surface for subsequent metal layer coverage. In addition, the use of oversized via's to minimize contact resistance, metal pitch (line width and spacing), and registration requirements for dense VLSI is very important.

Utilization of a composite low temperature polyimide-silicon dioxide layer will render the characteristics desired.

ORGANIC DIELECTRICS

The use of organic materials such as polyimides for interlevel dielectric offers numerous advantages over the conventional chemical-vapor-deposited doped oxides. Polyimide films of 0.5-5 μm thickness can be spun on a wafer like photoresist and have virtually planar surfaces. Improved device performance can be achieved by reduction of the interlevel lead capacitances. In addition, the conventional phosphorous-doped silane oxide requires reflow at temperatures as high as 1000°C after the deposition to achieve favorable contours if the oxide layer is very thick. In the case of polyimide, however, a final cure at temperatures as low as 250-300°C will render a dielectric layer having a dielectric strength of 100-300 V/μm, a dielectric constant of 3.0 to 3.4, a bulk resistivity of 10^{16} Ω·cm, and a pinhole density of less than 4 cm^{-2} and 0.1 cm^{-2} for 1- and 3-μm thick films, respectively. The completely cured (or imidized) form of polyimide is resistant to attack by all chemicals but hydrazine [1], hot bases, and plasma-excited oxygen. A simple method of patterning the polyimide other than using toxic and pyrophoric hydrazine [2] makes use of positive photoresist developers (strong bases) for etching partially cured polyimide and can be accomplished at the same time the positive resist layer is developed [3]. This procedure has been employed as a means of obtaining the results of this paper. These organic films have also been successfully patterned using dry processing techniques [4]. Polyimide protection against high humidity conditions [5], [6] and Na^+ diffusion [7] has also been reported.

NEW OXIDE DIELECTRIC

Recently a new low pressure oxide process has been reported which allows films to be deposited at temperatures in the range of 50-300°C [10]. This photochemical vapor-deposited oxide relies on neutral atomic oxygen being photogenerated from nitrous oxide by the application of ultraviolet light, and then reacting with silane to form a silicon dioxide layer. The electrical and mechanical qualities of this low temperature oxide (typically $\leq$200°C) are said to be better than or at least comparable to those of LPCVD [8] and plasma oxides [9]. The deposition rate of the photo-CVD silicon dioxide process is principally dependent on the intensity of the ultraviolet (UV) radiation source and typically ranges from 100-400 Å/min. This low deposition rate may prove detrimental to this process unless thin oxide layers are desired, as is the case in this paper.

OVERSIZED VIA's

Multilevel interconnect systems must provide for interlevel contact through holes or vias in the interlevel dielectric layers. In the design of a conventional two-level interconnection system which uses an oxide as the dielectric, a "nested via" is employed. Expanded first-level metal areas or pads under the via are used for two reasons: a) to provide a tolerance for the level-to-level registration at the via definition step and b) to provide an etch stop so that the passivation layer beneath the first-level metal is not attacked while etching the insulator

Manuscript received February 10, 1982; revised June 29, 1982. This work was sponsored in part under NASA Contract NAS8-33448.

The author is with the Microelectronics Research Laboratory, Mississippi State University, P. O. Box EE, Mississippi State, MS 39762.

0148-6411/82/1200-0516$00.75 © 1982 IEEE

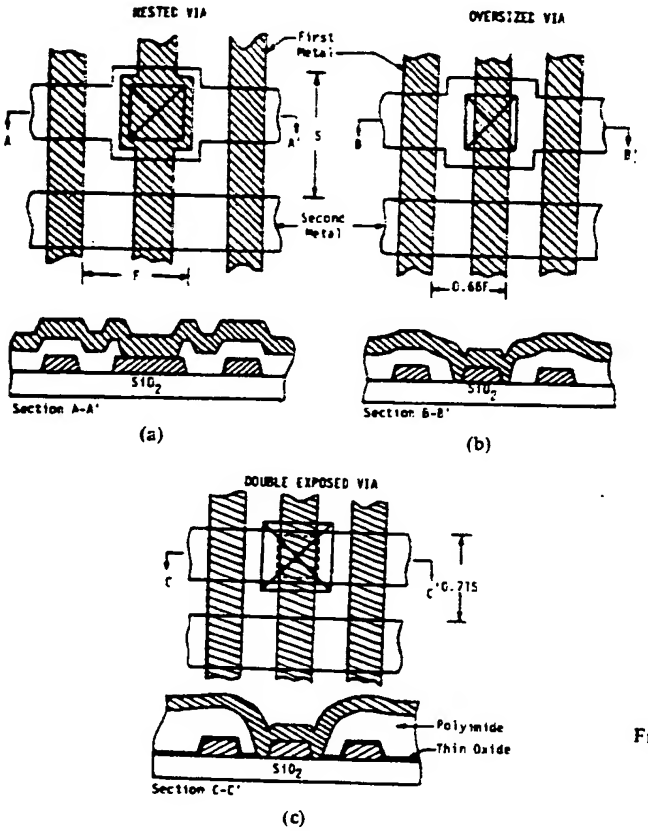

Fig. 1. Via interconnect layouts for increasing packing density. (a) Conventional nested via having enlarged first- and second-level metal. (b) "Oversized via" allowing increased packing density of first-level metal. (c) "Double etched via" allowing increased packing density for both metal levels (dotted outline indicates oxide-etch pattern).

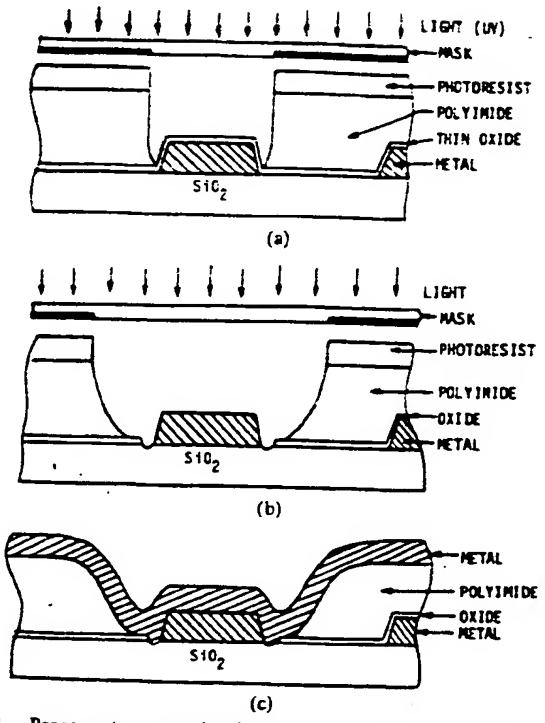

Fig. 2. Process steps associated with double-exposure procedure. (a) Small via mask opening to etch thin oxide layer. (b) Larger via mask opening to realize sloped contours and oversized via. (c) Deposition of second-level metal.

(SiO_2) for via formation. Also the second metal overlaps the via to protect the first-level metal during the second-level etching.

As seen in Fig. 1(a), in the conventional $Al/SiO_2/Al$ system—with nested vias – the Al pad is larger than the via on all four sides. Use of expanded metal pads increases the effective spacing between first-level leads and lowers the packing density. Furthermore, the placement of nested vias for a complex VLSI circuit make the chip layout operation somewhat more cumbersome. Absence of oversize pads for via locations are much more attractive for computer-aided designs of interconnection layout and they allow the maximum packing density of first-level interconnections permissible with patterning capabilities.

When polyimide is used as the interlevel dielectric, no attack of the underlying substrate material is experienced so that "oversized" vias as illustrated in Fig. 1(b) can be realized.

DOUBLE-EXPOSED POLYIMIDE/OXIDE DIELECTRIC

If a thin layer of low temperature oxide is deposited over the first level metal prior to applying the polyimide coating, then this thin oxide layer will act as an etch stop in patterning the second level metal for the "oversize" via case. This will alleviate the need for an overlapping second-level metal as shown in Fig. 1(c), thereby increasing the packing density of the second-level metal pattern also.

This thin low temperature oxide layer, which could very well be the photochemical vapor-deposited oxide mentioned previously, must be removed from the top of the first-level metal in the via such that ohmic contact may be established with the deposited second-level metal. Also, it is desirable to deposit a thick layer of polyimide dielectric in order to minimize capacitive coupling between metal levels. The etching of vias in the thick polyimide dielectric layer is a critical step. Sloped via sidewall contours are desirable in order to achieve continuity of the second-level metal. A method which allows removal of the thin oxide from the top of the first level metal and also forms the "oversized" via with sloped contours utilizes the "double exposure" process illustrated in Fig. 2. The method uses two via masking steps. The first step allows exposure of the photoresist and subsequent etching of the partially cured polyimide directly over the region for which the thin oxide layer is to be removed, as shown in Fig. 2(a). A dilute-buffered hydrogen-flouride (HF) solution is used to etch the exposed thin oxide layer with negligible effect to the polyimide layer and underlying substrate. Next a second via mask is used to expose a larger via area, resulting in the "oversized" via having contoured sidewalls as shown in Fig. 2(b). Finally, the second-level metal is deposited and patterned as shown in Figs. 2(c) and 1(c).

Also shown in Fig. 1 is an estimate of the interconnect space reduction capability which is realizable with the oversize via double exposure process. The first level metal spacing

F, present when via pads are used as shown in Fig. 1(a), is reduced by approximately 35 percent when the oversized via is introduced as shown in Fig. 1(b). In addition, the second level metal spacing S, shown in Fig. 1(a) when a second-level metal via pad is used is reduced by approximately 30 percent, as shown in Fig. 1(c).

In order to study the process variables involved in the double-exposure (and subsequent dielectric delineation) process, a layer of Dupont PI 2555 polyimide was deposited on a silicon wafer having 2000 Å of thermally grown SiO_2 on it. A smaller via test pattern mask was used to expose the AZ1350J photoresist on top of the polyimide layer and then the polyimide was etched at the same time the photoresist was developed. The wafer was then dipped in buffered HF solution to etch the SiO_2 layer and dehydrated. A second exposure is realized using a larger size via test pattern. Again, the photoresist and polyimide patterning occurs at the same time. The polyimide is then fully cured (imidized) and the results inspected using a scanning electron microscope as shown in Fig. 3. For this test run the process steps involved the following.

1) Wafer clean and oxidized.
2) Deposit Dupont VM651 coupler (0.02 percent in 95 percent methyl alcohol and five percent H_2O) or Hitachi coupler.
3) Spin deposit Dupont PI 2555 polyimide on wafer (final cured thickness of 0.5 to 1.0 μm).
4) Partially imidize at 100°C for 30 min.
5) Spin deposit Shipley AZ1350J at 6000 r/min.
6) Prebake photoresist at 90°C - 30 min.
7) Expose using small via mask in contact aligner.
8) Develop in Shipley AZ351, rinse and dehydrate at 50°C - five min.
9) Dip in BOE to etch oxide.
10) Rinse and dehydrate at 50°C-10 min.
11) Expose using large via mask.
12) Develop in AZ351.
13) Rinse and dehydrate at 50°C-5 min.

It should be noted that it is not necessary to use the double-exposure process in order to pattern the polyimide and the underlying thin oxide layer as shown in Fig. 2(c). The etching procedure could be reversed, i.e., pattern the thin oxide layer and then deposit the polyimide and pattern it. The reasons for not using this latter procedure are as follows.

a) Patterning the thin oxide layer first requires extra processing steps (i.e., deposit resist, prebake, mask alignment, develop and rinse, post-bake resist, etch oxide, strip resist, dehydrate, and then repeat the process for the polyimide layer).
b) It is found that by using the process illustrated in Fig. 2, often good ohmic contact between first- and second-level metal in the via can be obtained without the need for a "back sputter" clean up step just prior to depositing the second-level metal. This back sputtering can be detrimental to circuit performance, especially for metal oxide semiconductor (MOS) type technologies. In the reverse process, however, when polyimide contacts the first-level metal (through the patterned thin oxide) during the precure (preimidize) stages before patterning, a back sputter clean up step is almost always required in order to gain continuity between metal levels. It is believed that the polyimide resin reacts with the aluminum (or aluminum oxide) to form an "invisible shield" which cannot be easily penetrated with wet chemicals [11].

Fig. 3. Scanning electron micrograph of test wafer illustrating the double-exposure oxide-etch process. Small via mask oxide etch dimension is 3 μm and larger via mask polyimide etch dimension is 5 × 8 μm.

As illustrated in Fig. 1(c), the use of polyimide as an interlevel dielectric allows a much thicker dielectric to be realized without encountering severe tensile stresses which are commonly characterized by other dielectric materials [12]. As mentioned, a thicker dielectric is highly desirable in terms of decreasing capacitive coupling effects between metal levels.

A scanning electron microscope (SEM) micrograph showing the cross section of one side of the large mask via is illustrated in Fig. 4 to demonstrate the sidewall slopes attainable in thick (2 μm) polyimide films. Metal step coverage over such thick layer edges is very good so long as adequate slopes are realized. While Dupont variety polyimide (PI-2555) was used for this particular test wafer, Hitachi PIQ-13 has also been investigated and yields similar results.

In Fig. 5, a cross section of a double-exposed via is shown after deposition of the second-level metal. Very good step coverage is obtained here by using a 1 μm thick Al/Si metal layer and 1.5-2 μm thick polyimide. The thin CVD oxide used as an etch stop in patterning the second-level metal is approximately 1500 Å thick. Contact resistance for a 5 X 5 μm small via mask dimension is approximately 250 milliohms per via for 7 μm wide interconnect.

CONCLUSION

A new process for double-layer metal interconnect via formation has been investigated with the following results: A very low temperature process if the photochemical vapor deposited oxide is used with polyimide as the interlayer dielectric

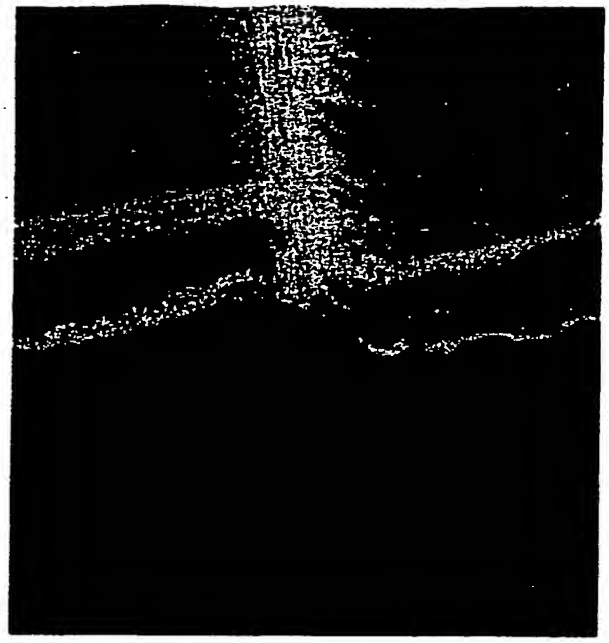

Fig. 4. Slope of via sidewall for thick (2 μm) polyimide layer indicating step coverage realized.

material, a decrease in capacitive coupling effects for thick polyimide layers, an increase in packing density for both first- and second-level metal layers, the absence of oversized metal pads for vias to facilitate computer-aided design techniques, and a process which can be realized using either wet chemical or dry plasma processing. It is hoped that this process will assist in promoting future VLSI circuitry to even higher densities.

REFERENCES

[1] J. I. Jones, "The reactions of hydrazine with polyimides and its utility," *J. Polym. Sci.*, vol. 22, p. 773, 1969.

[2] S. Horie *et al.*, "The development of planar chrome IC's with two-level interconnection," Report of the Japan Commun. Soc., Sym. of the S.C. Group, no. 90, 1977–78.

Fig. 5. SEM micrograph of double-exposed via after deposition of second-level metal. Second-level metal is approximately 1 μm thick, 7 μm wide. First-level metal is 1 μm thick, 5 μm wide.

[3] J. C. Yen, in *Proc. Electrochemical Society Meeting*, Spring 1975, vol. 75–1, Abs. 170, 1975.

[4] J. M. Moran and D. Maydan, *Bell Syst. Tech. J.*, vol. 58, p. 1027, 1979.

[5] S. Miller, "A technique for passivating thin film hybrids," *Circuit Manufacturing*, pp. 54–58, April 1977.

[6] A. Saika, K. Mukai, S. Takakushi, K. Yamanaka, and S. Harada, "Reliability of semiconductor devices using a resin insulation structure," *Central Research Laboratory Tech. Bull.*, Hitachi, Ltd.

[7] S. Harada, K. Sato, A. Saiki, T. Kimura, T. Okubo, and K. Mukai, "Two level construction of transistor electrodes," *Japan J. Appl. Phys.*, vol. 44, p. 297, 1974.

[8] P. J. Tobin, J. B. Price, and L. M. Campbell, "Low pressure CVD of phosphosilicate glass," Electrochemical Society Meeting, Recent New Abstract, Spring 1977.

[9] M. Vanderberg, "Properties of plasma deposited silicon oxide," Electrochemical Society, Abstract No. 99, Spring 1979 Meeting.

[10] J. W. Peters, "Low temperature photo-CVD oxide processing for semiconductor device applications," *International Electron Devices Meet. Tech. Dig.*, pp. 240–243, Washington, DC, Dec. 7–9, 1981.

[11] J. I. Bowers, E. I. Dupont, Co., private communications.

[12] K. Mukai *et al.* "Planar multilevel interconnect technology employing polyimide," *J. of Solid State Ckts*, vol. SC-13, no. 4, p. 462, Aug. 1978.

IEEE TRANSACTIONS ON

COMPONENTS, HYBRIDS, AND MANUFACTURING TECHNOLOGY

DECEMBER 1982 VOLUME CHMT-5 NUMBER 4 (ISSN 0148-6411)

A PUBLICATION OF THE IEEE COMPONENTS, HYBRIDS, AND MANUFACTURING TECHNOLOGY SOCIETY